Atomic Layer Etching of Si(100) for Reducing Etching Damage

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Atomic layer etching is very important for fabrication VLSI devices as well as future nano-scale devices. The atomic layer etching process is basically a self-limited process that enables to attain the precise control of etching depth and minimization of etching damage[1]. As the feature length of devices shrinks further in the future, it is expected that the atomic layer processing should gain more attention.

Atomic layer etching of Si(100) was carried out using a sequential Cl_2 adsorption and Ar^+ ion irradiation. Ar^+ ion was generated by high-density helicon plasma and ICP-type ion source. The sequence of etching process is the following 4 steps: (1) adsorption of Cl_2 on Si surface; (2) evacuation; (3) Ar^+ ion irradiation to the surface; (4) evacuation. The sequence is shown schematically in Fig.1. The atomic layer etching apparatus is equipped with an Ar^+ ion generation source, a high-speed automatic shutter, a high-speed automatic valve, and an additional RF power to bias the susceptor. The process parameters for optimizing the atomic layer etching characteristics are Cl_2 gas exposure duration, Ar^+ ion irradiation duration, Ar^+ ion energy, etc. The typical experimental conditions are listed in Table 1.

It is expected that the atomic layer etching of Si(100)should be limited to 0.68nm per cycle, which corresponds to the half mono-layer thickness of silicon[2]. By using low energy Ar^+ ions slightly above the threshold energy for Si etching, the low damage etching of Si could be possible. Even though the etch rate is quite low compared to the conventional plasma etching processes, the atomic layer etching process has advantage of strict control of depth as well as the low etch damage. In this work, we reports the self-limited etching of (100) silicon at room temperature and the advantages of the process on reduction of etch damage.

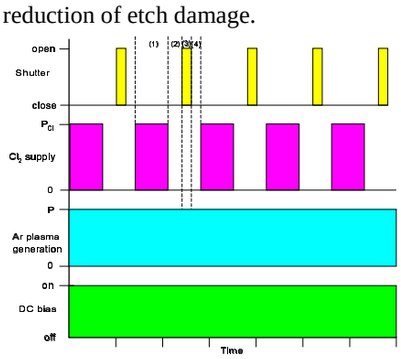

Fig. 1. Schematic diagram of etching process. (1) adsorption of Cl_2 on Si surface; (2) evacuation; (3) Ar^+ ion irradiation to the surface; (4) evacuation.

Table 1. Typical experimental parameters.

R.F. power	50W
Ar flow rate	5sccm
Cl_2 flow rate	0.5sccm
Cl_2 valve open time	1~30sec
Shutter open time	1sec
Bias at substrate	-35V

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References

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